



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/672,637	09/28/2000	Gary Dan Dotson	00AB152	8211
7590	12/01/2004			EXAMINER
Allen-Bradley Company, Inc. Attention: John J. Horn Patent Dept./704P Floor 8 T-29 1201 South Second Street Milwaukee, WI 53204			LEE, HWA C	
			ART UNIT	PAPER NUMBER
			2672	
			DATE MAILED: 12/01/2004	

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/672,637	DOTSON ET AL.	
	Examiner	Art Unit	
	Hwa C Lee	2672	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 01 July 2004.
- 2a) This action is **FINAL**. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-4 and 9-20 is/are rejected.
- 7) Claim(s) 5-8 is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____. |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____. | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| | 6) <input type="checkbox"/> Other: _____. |

DETAILED ACTION

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claim 1 is provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of copending Application No. 10/929837. Although the conflicting claims are not identical, they are not patentably distinct from each other because the conflicting claims are identical except for the limitation directed to a logic device, and said logic device as recited in Application No. 10/929837 comprises the same limitations using slightly different language.

3. This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

4. Claim 1 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6,734,866. Although the conflicting claims are not identical, they are not patentably distinct from

each other because both claims are directed to a raster engine for displaying a plurality of display modes corresponding to a plurality of disparate displays. Said multiplexer recited in Patent No. 6,734,866 specifically is a logic device. In addition, said pixel shift logic system recited in Patent No. 6,734,866 specifically comprises a parallel output as recited in the instant claim.

5. Claim 2 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 2 of U.S. Patent No. 6,734,866. Although the conflicting claims are not identical, they are not patentably distinct from each other because all limitations added in the dependent claim 2 are exactly the same in the conflicting claim 2 of U.S. Patent No. 6,734,866.

6. Claim 3 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 3 of U.S. Patent No. 6,734,866. Although the conflicting claims are not identical, they are not patentably distinct from each other because all limitations added in the dependent claim 3 are exactly the same in the conflicting claim 3 of U.S. Patent No. 6,734,866.

7. Claims 4 and 19 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6,734,866. Although the conflicting claims are not identical, they are not patentably distinct from each other because of the same reasoning as applied to claim 1 above.

8. Claim 5 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 6 of U.S. Patent No. 6,734,866. Although the conflicting claims are not identical, they are not patentably distinct from

each other because all limitations added in the dependent claim 5 are exactly the same in the conflicting claim 6 of U.S. Patent No. 6,734,866.

9. Claim 6 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 7 of U.S. Patent No. 6,734,866. Although the conflicting claims are not identical, they are not patentably distinct from each other because all limitations added in the dependent claim 6 are exactly the same in the conflicting claim 7 of U.S. Patent No. 6,734,866 except for the language, "whereby improved color intensity range is provided". It is well known in the art, however, that said copying most significant bits from selected pixels data into corresponding unused least significant bits specifically improves the color intensity range. Thus the two conflicting claims are directed to the same limitations.

10. Claim 7 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 8 of U.S. Patent No. 6,734,866. Although the conflicting claims are not identical, they are not patentably distinct from each other because all limitations added in the dependent claim 7 are exactly the same in the conflicting claim 8 of U.S. Patent No. 6,734,866.

11. Claim 8 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 8 of U.S. Patent No. 6,734,866. Although the conflicting claims are not identical, they are not patentably distinct from each other because all limitations added in the dependent claim 8 are exactly the same in the conflicting claim 8 of U.S. Patent No. 6,734,866. Also see rejections for claims 1 and 4 above.

12. Claim 9 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 9 of U.S. Patent No. 6,734,866. Although the conflicting claims are not identical, they are not patentably distinct from each other because all limitations added in the dependent claim 9 are exactly the same in the conflicting claim 9 of U.S. Patent No. 6,734,866.

13. Claim 10 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 13 of U.S. Patent No. 6,734,866. Although the conflicting claims are not identical, they are not patentably distinct from each other because the display mode as recited in claims 1 and 13 in U.S. Patent No. 6,734,866 specifically is defined by as comprising a color mode, a shift mode, and a pixel mode (Col. 8, lines 38-52). The examiner realizes that although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

In this situation, the claims of U.S. Patent No. 6,734,866 is read in light of the specification in order to clarify the definition of "display mode."

14. Claim 15 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 15 of U.S. Patent No. 6,734,866. Although the conflicting claims are not identical, they are not patentably distinct from each other because the limitations are nearly identical and directed to the same limitations regarding resolution and refresh rates of the pixel mode.

15. Claim 17 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 14 of U.S. Patent No. 6,734,866.

Art Unit: 2672

Although the conflicting claims are not identical, they are not patentably distinct from each other because the limitations are nearly identical directed to the resolution and refresh rates of the shift mode.

16. Claim 20 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 19 of U.S. Patent No. 6,734,866.

Although the conflicting claims are not identical, they are not patentably distinct from each other because all limitations added in the dependent claim 20 are exactly the same in the conflicting claim 19 of U.S. Patent No. 6,734,866.

Claim Rejections - 35 USC § 103

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

18. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Art Unit: 2672

19. Claims 1-3, 9-17 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reddy et al., U.S. Patent No.: 6,215,459 in view of Ramamurthy, US Patent No.: 6,189,082, and further in view of Boger, U.S. Patent No.: 6,326,935.

20. In regards to claim 1, the limitations recited in the preamble (raster engine) are not given patentable weight. Never the less, Reddy et al. specifically teaches a video controller, which specifically comprises a raster engine since all video controller must contain a raster engine.

21. Reddy et al. teaches a video controller for controlling at least two video displays (Col. 4, lines 7-32). Said video controller allows for displaying two different images on a separate displays at the same time, wherein the resolution and the refresh rate is the same for both displays (FIG. 1-2 and Col. 4, line 60 – Col. 5, line 12) or different (FIG. 7-9 and Col. 7, line 50 – Col. 12, line 7). Said video controller comprises a video memory (108), memory controller (101), attribute controller (102), and a look-up table (103). Reddy et al. teaches flip-flop latches (logic devices) (FIG. 2, No. 210 and 211), which clearly have parallel outputs for outputting the video data obtained from the video memory (108) via the attribute controller (102) and the look-up table (103). Said parallel output provides the appropriate video data in proper display mode corresponding to the plurality of displays (Col. 6, line 9 – Col. 7, line 22). Said proper pixel data corresponding to the display mode must remap said pixel data in order to display said pixel data in respective display units. Displaying the pixel data on a plurality of displays specifically is remapping pixel data. In addition, Reddy et al. explicitly teaches memory map (FIG. 3 and Col. 5, lines 28-59) for displaying the pixel data. Further, said

Art Unit: 2672

corresponding video data in respective video modes are sent to a plurality of displays (flat panel and CRT) via the flat panel controller and DAC, which specifically are universal routing schemes applicable to said plurality of displays.

22. In addition, Reddy et al. teaches said attribute controller generating pixel data (251) in a format of 1, 2, 4 or 8 bits per pixel from video data stored in video memory, which specifically are different display modes, and thus said attribute controller specifically is at least one control register. Although Reddy et al. does not explicitly teach a programmable control register, said attribute register must be programmable via the graphics driver in order to display different resolutions on each displays as described above. In addition, it is well known in the art to implement a programmable control register.

23. An analogous art, Ramamurthy, US Patent No.: 6,189,082 teaches a well known programmable controller chip, wherein a graphics controller can be programmed with the display resolution corresponding to the display monitor (Col. 1, lines 18 – Col. 2, line 19). Software such as BIOS or graphics drivers can program the controller chips by writing appropriate values to the registers in order to accommodate the respective display. It would have been obvious to one of ordinary skill in the art at the time of the invention to take the teachings of Reddy et al. and to add from Ramamurthy, the programmable graphics controller in order to automatically allow the graphics driver to select the proper resolution to display depending on the application. Thus, said programmable control register allows easy conversion of display data for displaying on a plurality of display types.

Art Unit: 2672

24. Reddy et al. teaches a video memory as described above, but does not explicitly teach a dual port RAM device. It is well known in the art, however, that a video RAM (DRAM, SDRAM, etc.) specifically is a dual port RAM, and it is likewise well known in the art that video RAM is used in a graphics system.

25. An analogous art, Boger teaches a display apparatus capable of displaying a television interlaced mode and a computer non-interlaced mode (Col. 2, lines 1-18), which specifically are displaying a plurality of display modes. Said display apparatus comprises a video memory comprising VRAM, SGRAM, WRAM and the like (Col. 4, lines 38-65 and Col. 5, line 44 – Col. 6, line 50). Said display device is capable of displaying a CRT, LCD, LED, PALC, and HGED, which are require different display modes. In addition, said video RAM specifically function as the frame buffer, and thus a dual port RAM inherently operates to obtain pixel data from the frame buffer. Further, Reddy et al. teaches a video RAM for storing video frames. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to take the teachings of Reddy et al. and Ramamurthy and to add from Boger the dual port RAM as the video RAM since said dual port RAM is the standard video RAM used in the art. The motivation to combine the arts is simply the fact that a dual port RAM is the accepted device to use as a video RAM in the art today, and it would be obvious to use a standard, state of the art technology in the art.

26. In regards to claim 2, Reddy et al. teaches a 2x clock for displaying pixel data in a format of 1, 2, 4 or 8 bits per pixel (Col. 5, lines 13-28). Said 2x clock specifically is two pixels per clock. Since the applicant recites the “one of” language, Reddy et al.

reads on the limitations of the instant claim. In addition, the rest of the display mode as recited in the instant claim are standard display modes corresponding to a plurality of display devices and are comparable to said display more as taught by Reddy et al. Thus, Reddy et al. teaches all limitations of the instant claim.

27. In regards to claims 3 and 9, Reddy et al. explicitly teaches a look-up table (FIG. 2), wherein the logic device receives the selected pixel data form the dual port RAM device via the look-up table as applied to claim 1 above.

28. In regards to claim 10, Reddy et al. Ramamurthy and Boger teach the raster engine of claim 1. In addition, Reddy et al. explicitly teaches a plurality of pixel modes and a 256 color mode comprising a look-up table mode as applied to claims 1-3 above. Reddy et al. also teaches a 2x clock, which specifically is a 2 pixels per pixel clock shift mode as applied to claims 1-3 above.

29. In regards to claim 11, the same basis and rationale for claim rejection as applied to claims 3 and 10 above. Reddy et al. explicitly teaches a look-up table.

30. In regards to claims 12 and 16-17, the same basis and rationale for claim rejection as applied to claim 10 above. Reddy explicitly teaches 2X clock, which specifically is 2 pixels per shift clock.

31. In regards to claims 13-15, the same basis and rationale for claim rejection as applied to claims 1-3 above. Reddy et al. explicitly teaches 1, 2, 4, or 8 bits per pixel.

32. In regards to claim 20, Reddy et al., Ramamurthy and Boger teaches the raster engine of claim 1. In addition, Boger explicitly teaches a user interface for selecting a display mode (Col. 6, line 62 – Col. 7, line 23), which specifically is a direct display

command interface. It would have been obvious to one of ordinary skill in the art at the time of the invention to take the teachings of Reddy et al., Ramamurthy and to add from Boger, the user interface executed by a software in order to allow the user a direct access to changing the display mode. This allows the user to adjust and change the display mode by providing the input data concerning the display units, which maybe required depending on the usage.

33. Claims 4 and 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reddy et al. in view of Ramamurthy, and further in view of Boger, and further in view of Schindler et al., U.S. Patent No.: 6,516,467.

34. In regards to claims 4 and 18-19, Reddy, Ramamurthy and Boger teach the raster engine of claims 1 and 3, but do not explicitly teach ***wherein the logic device comprises a multiplexer***. It is well known in the art, however, that a multiplexer can easily substitute for a flip-flop, especially when selecting from a plurality of inputs and outputting to a plurality of outputs. Hence the inherent function of a multiplexer, and thus it would have been obvious to one or ordinary skill in the art to substitute a multiplexer for the flip-flop in order to output a plurality of display modes to a plurality of display types.

35. An analogous art, Schindler et al. teaches a home entertainment system with a plurality of input signals, wherein the proper video display is output to the display unit through a multiplexer (Col. 11, line 58 - Col. 12, line 42 and FIGS. 5-7). It would have been obvious to one of ordinary skill in the art at the time of the invention to take the teachings Reddy et al. and Ramamurthy et al. and to modify the flip-flop with the

multiplexer as taught by Schindler et al. in order to implement standard logic device when choosing from a plurality of input signals (different display modes) and outputting the appropriate signal to the corresponding output devices (display units). A multiplexer has an advantage over a flip-flop that it allows for a larger number of inputs and outputs, which means, one multiplexer may replace several flip-flops.

Allowable Subject Matter

36. Claims 5-8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

37. The following is a statement of reasons for the indication of allowable subject matter: In regarding claim 5, the applicant recites a logic device adapted to provide the selected pixel data to the output device in a 24 bit parallel format when the selected display mode is one of single 16 bit 565 pixel per clock and single 16 bit 555 pixel per clock. While it is well known in the art to display in a 24 bit parallel format, the prior art of record do not teach displaying in said 24 bit parallel format when selecting a single 16 bit 565/555 pixel per clock mode, which would be required in order to display the proper display mode corresponding to the selected output device. In regarding claim 6, the prior art of record do not teach copying a plurality of most significant bits from the selected pixel data into a corresponding plurality of unused least significant bit in the 24 bit parallel format in order to improved color intensity range. In regards to claims 7-8,

Art Unit: 2672

said added limitations are taught by prior art of record, but said claims are allowable only because they depend from claims 5 and 6.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hwa C Lee whose telephone number is 703-305-8987. The examiner can normally be reached on M-F 8:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Razavi can be reached on 703-305-4713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hwa C Lee
Examiner
Art Unit 2672

HCL
11/28/04

Application/Control Number: 09/672,637
Art Unit: 2672

Page 14



MICHAEL RAZAVI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800